EE 435

Lecture 4

Spring 2021

Fully Differential Single-Stage Amplifier Design

- General Differential Analysis
- 5T Op Amp from simple quarter circuit
- Biasing with CMFB circuit
- ⇨ Common-mode and differential-mode analysis
- ⇨ Common Mode Gain
- ⇨ Overall Transfer Characteristics

Design of 5T Op Amp

Slew Rate

Review from last lecture:

Where we are at:

Basic Op Amp Design

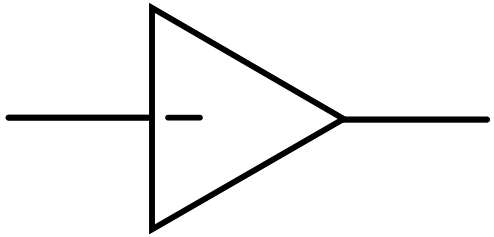
- Fundamental Amplifier Design Issues
- Single-Stage Low Gain Op Amps
- Single-Stage High Gain Op Amps
- Two-Stage Op Amp
- Other Basic Gain Enhancement Approaches

Review from last lecture:

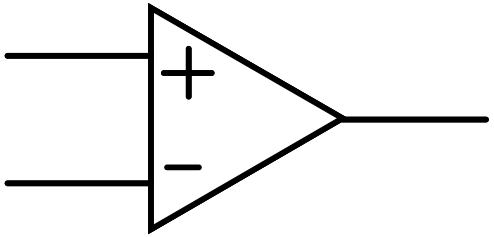
Where we are at:

Single-Stage Low-Gain Op Amps

- Single-ended input



- Differential Input



(Symbol does not distinguish between different amplifier types)

Review from last lecture:

Differential Input Low Gain Op Amps

Will Next Show That :

- Differential input op amps can be readily obtained from single-ended op amps

- Performance characteristics of differential op amps can be directly determined from those of the single-ended counterparts

Review from last lecture:

Counterpart Networks

Definition: The counterpart network of a network is obtained by replacing all n-channel devices with p- channel devices, replacing all p-channel devices with n-channel devices, replacing V_{SS} biases with V_{DD} biases, and replacing all V_{DD} biases with V_{SS} biases.

Review from last lecture:

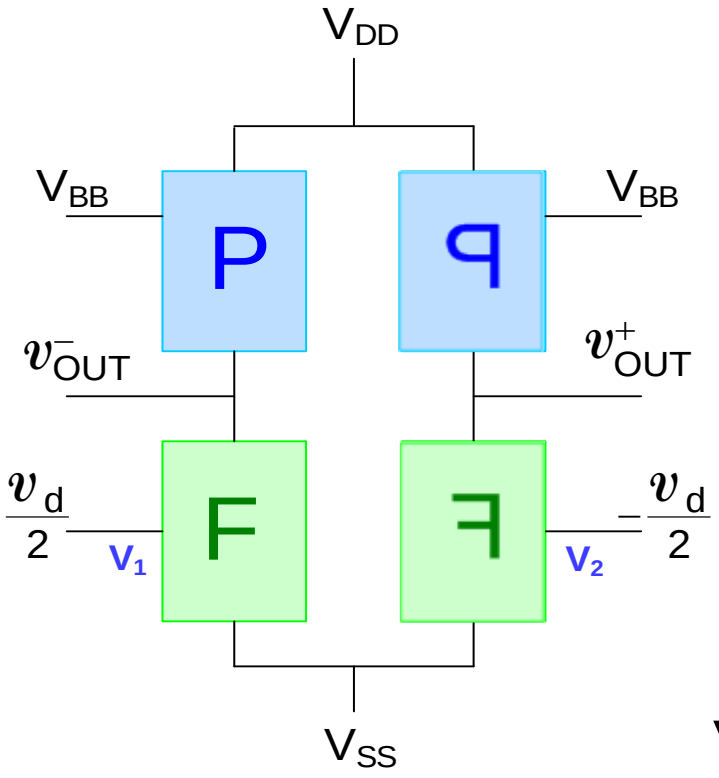
Counterpart Networks

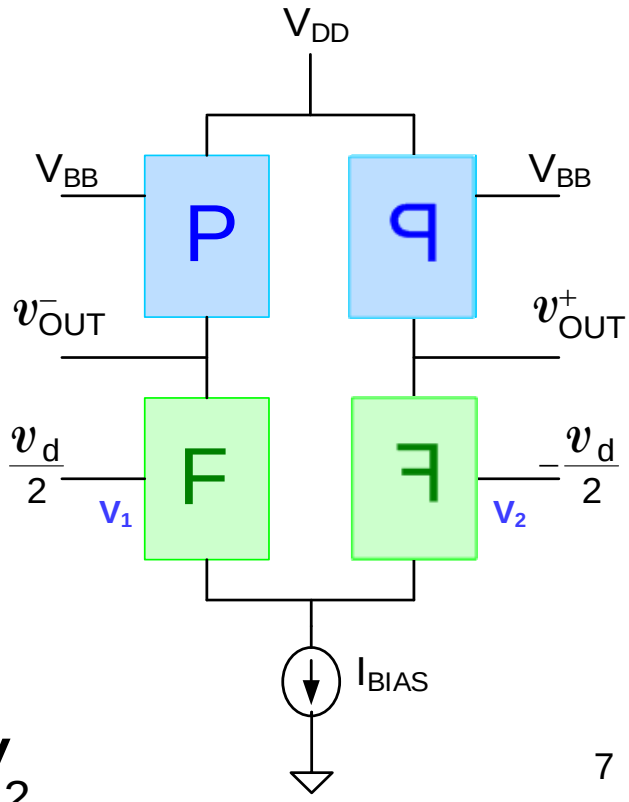
Theorem: The parametric expressions for all small-signal characteristics, such as voltage gain, output impedance, and transconductance of a network and its counterpart network are the same.

Synthesis of fully-differential op amps from symmetric networks and counterpart networks

Theorem: If F is any network with a single input and P is its counterpart network, then the following circuits are fully differential circuits --- "op amps".

Review from last lecture:



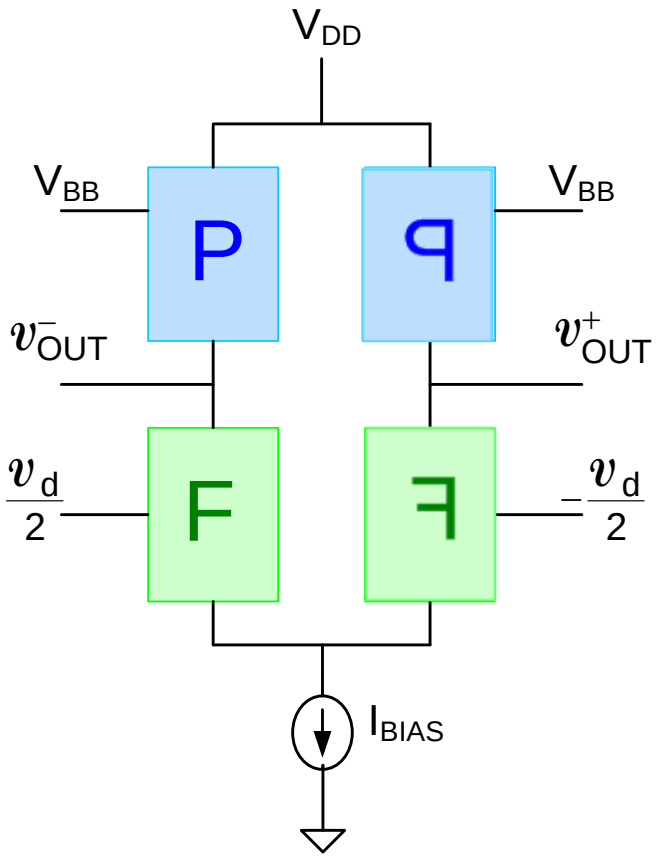


$$V_d = V_1 - V_2$$

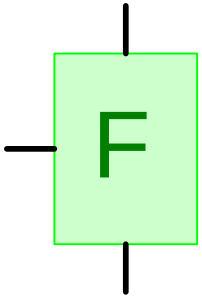
Synthesis of fully-differential op amps from symmetric networks and counterpart networks

Review from last lecture:

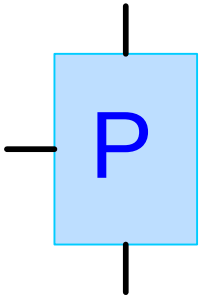
Terminology



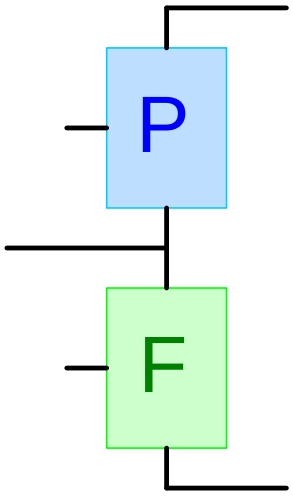
$$V_d = V_1 - V_2$$



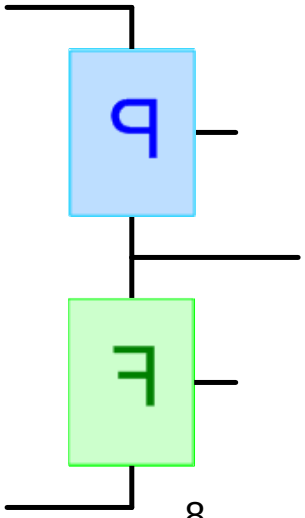
Quarter Circuit



Counterpart Circuit



Half Circuit

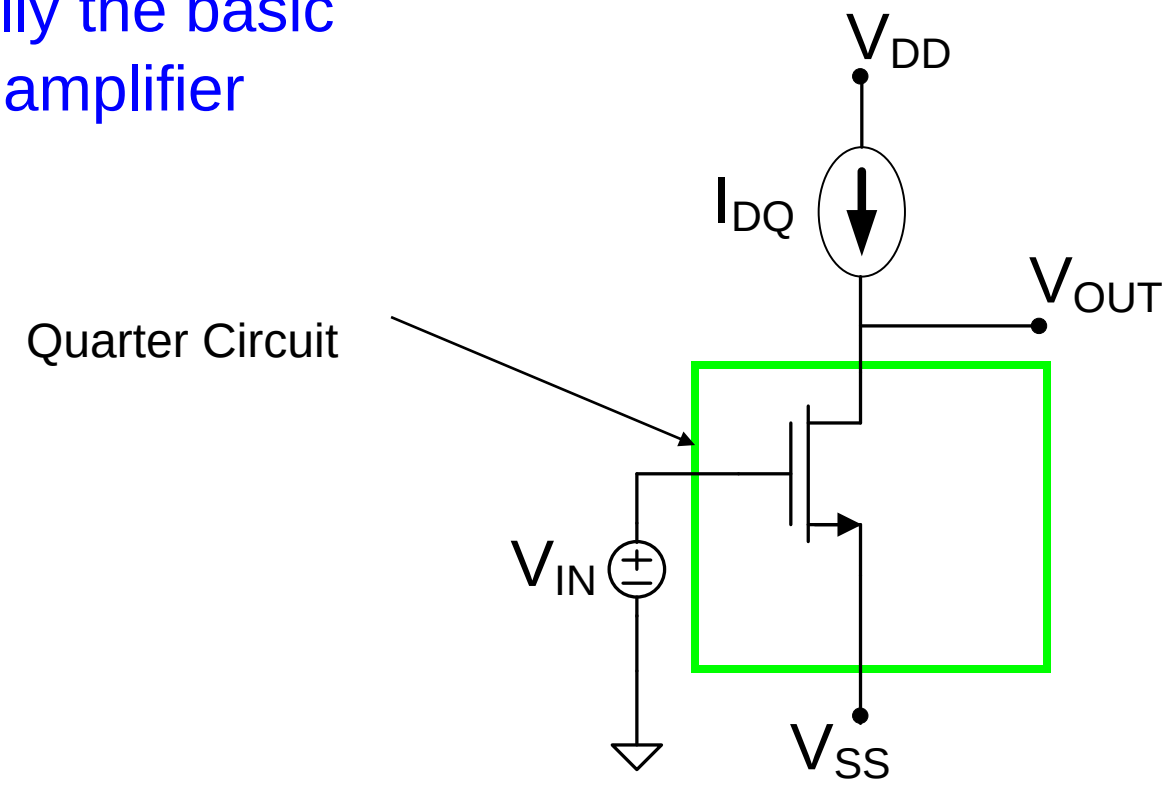


Symmetric Half Circuit

Review from last lecture:

Applications of Quarter-Circuit Concept to Op Amp Design

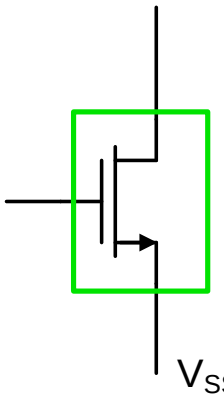
consider initially the basic single-ended amplifier



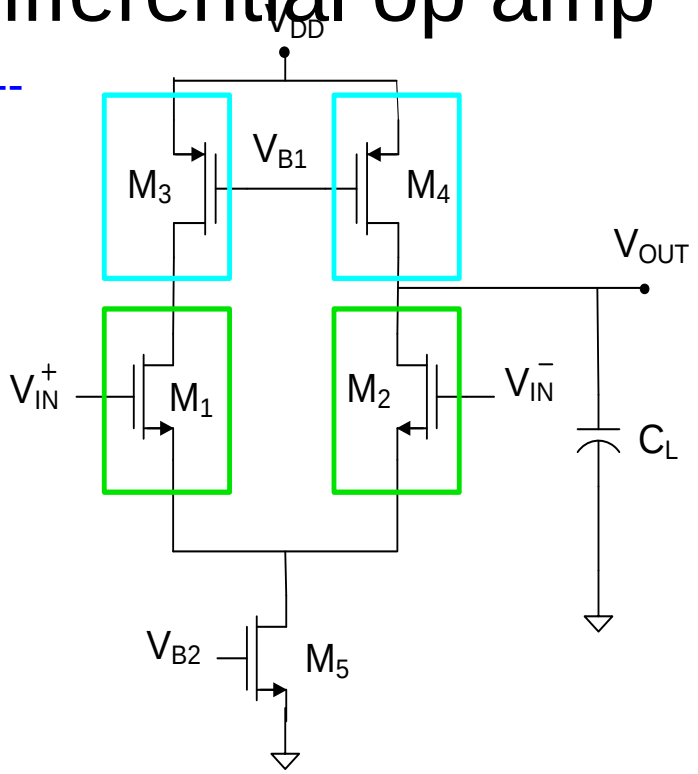
Review from last lecture:

Single-stage low-gain differential op amp

-- The "differential" gain --



Quarter Circuit



Single-Ended Output : Differential Input Gain

$$A(s) = \frac{v_{OUT}}{v_d} = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{o1} + g_{o3}}$$

$$A_{V0} = \frac{-g_{m1}}{2(g_{o1} + g_{o3})}$$

$$BW = \frac{g_{o1} + g_{o3}}{C_L}$$

$$GB = \frac{g_{m1}}{2C_L}$$

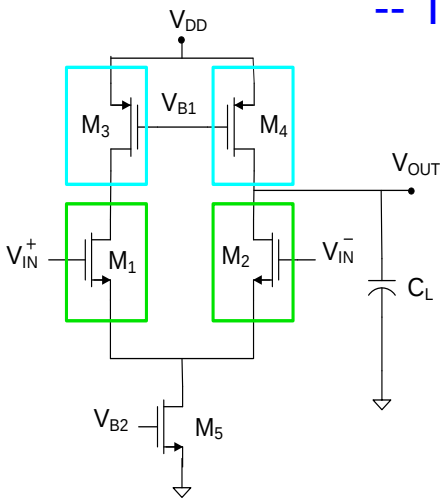
Circuit is Very Sensitive to V_{B1} and V_{B2} !!

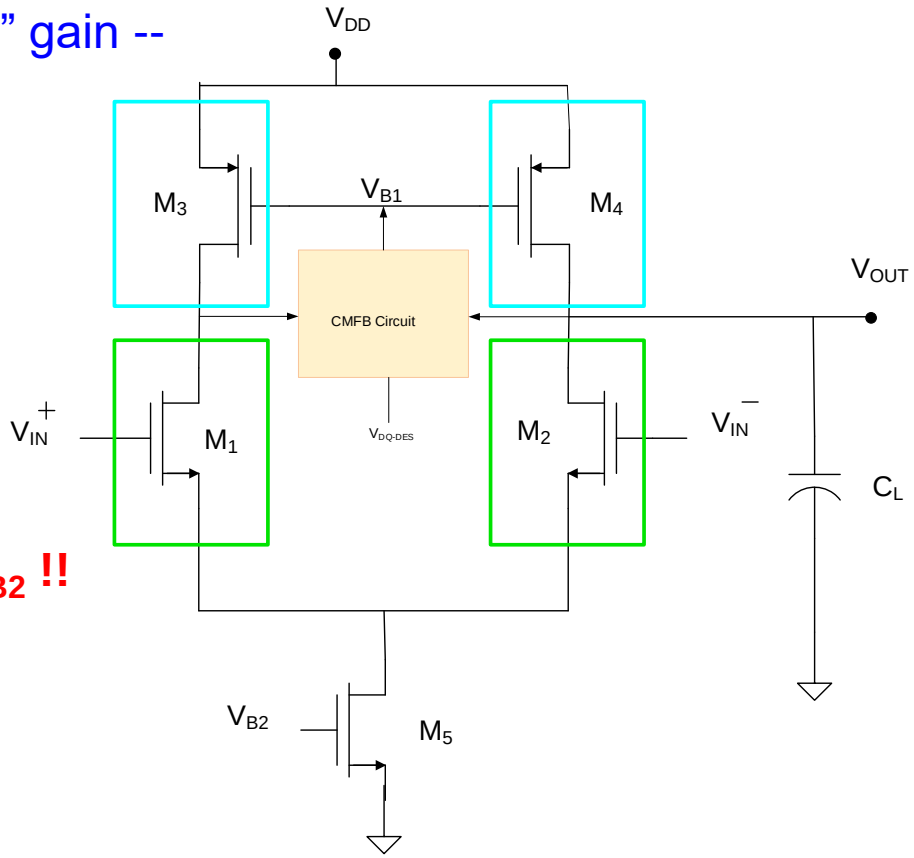
- Have synthesized fully differential op amp from quarter circuit !
- Have obtained analysis of fully differential op amp directly from quarter circuit !
- Still need to determine what happens if input is not differential !
- **Have almost obtained op amp characteristics by inspection from quarter circuit !!**

Review from last lecture:

Single-stage low-gain differential op amp

-- The “differential” gain --





Need CMFB circuit to establish V_{B1} or V_{B2} !!

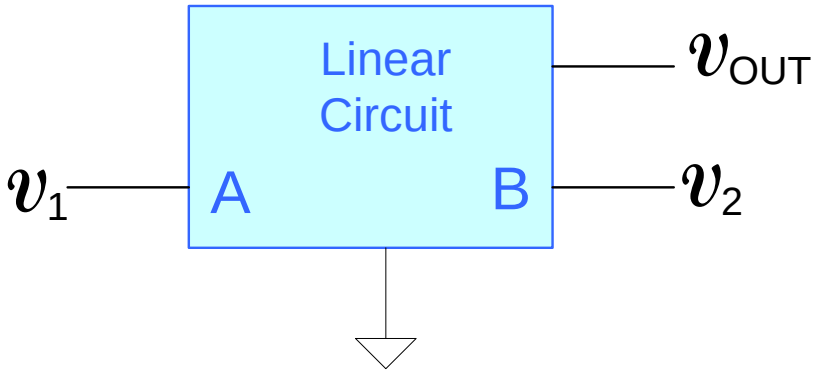
- CMFB circuit determines average value of the drain voltages
- Compares the average to the desired quiescent drain voltages
- Established a feedback signal V_{B1} to set the right Q-point
- Shown for V_{B1} but could alternately be applied to V_{B2}

Details about CMFB circuits will be discussed later

- Fully Differential Single-Stage Amplifier D
  - General Differential Analysis
  - 5T Op Amp from simple quarter circuit
  - Biasing with CMFB circuit
  - Common-mode and differential-mode analysis
  - Common Mode Gain
  - Overall Transfer Characteristics
- Design of 5T Op Amp
- Slew Rate

Common-Mode and Differential-Mode Analysis

Consider an output voltage for any linear circuit with two inputs
(i.e. need not be symmetric)



By superposition

$$v_{OUT} = A_1 v_1 + A_2 v_2$$

where A_1 and A_2 are the gains (transfer functions) from inputs 1 and 2 to the output respectively

Define the common-mode and difference-mode inputs by

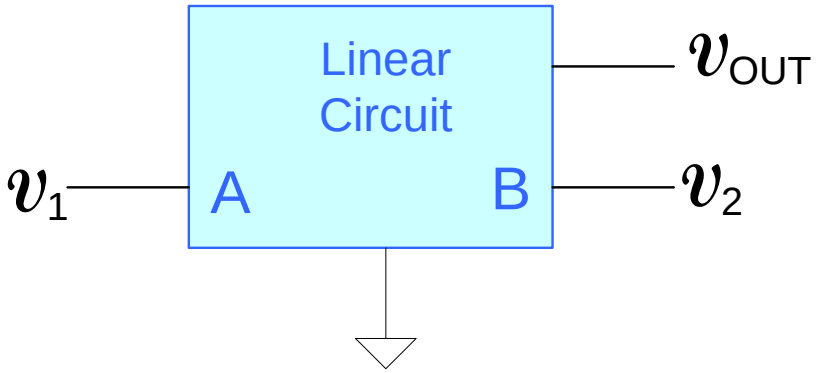
$$v_c = \frac{v_1 + v_2}{2} \qquad v_d = v_1 - v_2$$

These two equations can be solved for v_1 and v_2 to obtain

$$v_1 = v_c + \frac{v_d}{2} \qquad v_2 = v_c - \frac{v_d}{2}$$

Common-Mode and Differential-Mode Analysis

Consider an output voltage for any linear circuit with two inputs



$$v_{OUT}=A_1 v_1+A_2 v_2$$

Substituting into the expression for v_{OUT}, we obtain

$$v_{OUT}=A_1\left(v_c+\frac{v_d}{2}\right)+A_2\left(v_c-\frac{v_d}{2}\right)$$

Rearranging terms we obtain

$$v_{OUT}=v_c\left(A_1+A_2\right)+v_d\left(\frac{A_1-A_2}{2}\right)$$

If we define A_c and A_d by

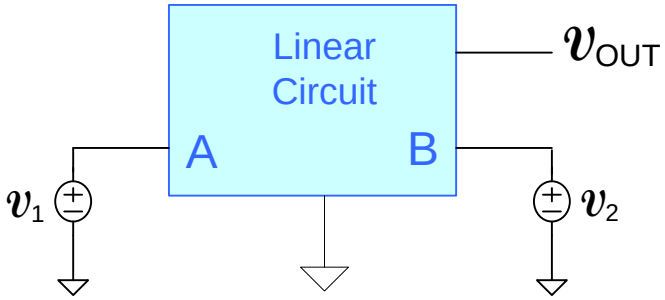
$$A_c=A_1+A_2 \qquad A_d=\frac{A_1-A_2}{2}$$

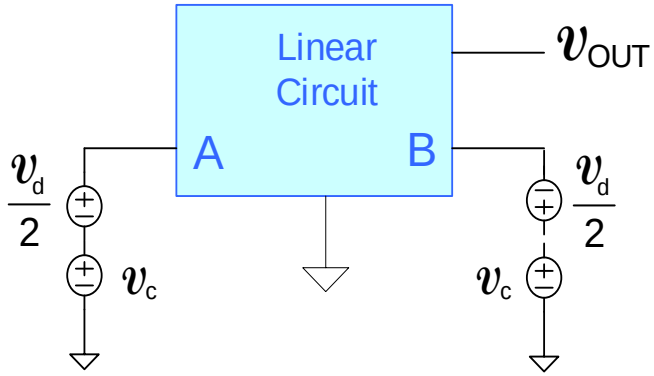
Can express v_{OUT} as

$$v_{OUT}=v_c A_c+v_d A_d$$

Common-Mode and Differential-Mode Analysis

Depiction of singe-ended inputs and common/difference mode inputs



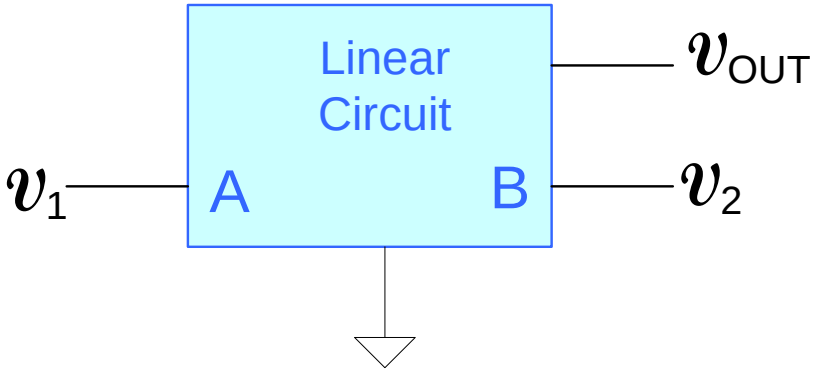


$$v_{OUT}=A_1 v_1+A_2 v_2 \quad \Longleftrightarrow \quad v_{OUT}=v_c A_c+v_d A_d$$

- Applicable to any linear circuit with two inputs and a single output
- Op amps often have symmetry and this symmetry further simplifies analysis

Common-Mode and Differential-Mode Analysis

Consider <u>any</u> output voltage for any linear circuit with two inputs



$$A_c = A_1 + A_2$$

$$A_d = \frac{A_1 - A_2}{2}$$

$$v_{OUT} = A_1 v_1 + A_2 v_2$$

$$v_{OUT} = v_c A_c + v_d A_d$$

$$v_{OUT} = v_c (A_1 + A_2) + v_d \left(\frac{A_1 - A_2}{2} \right)$$

Implication: Can solve any linear two-input circuit by applying superposition with v_1 and v_2 as inputs or with v_c and v_d as inputs. This can be summarized in the following theorem:

Theorem 1: The output for any linear network can be expressed equivalently as $v_{OUT} = A_1 v_1 + A_2 v_2$ or as $v_{OUT} = v_c A_c + v_d A_d$
Superposition can be applied to either v_1 and v_2 to obtain A_1 and A_2 or to v_c and v_d to obtain A_c and A_d

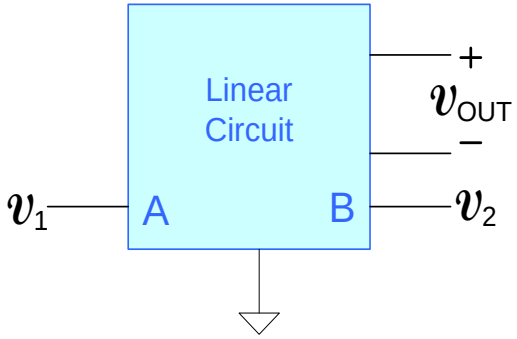
Observation: In a circuit with $A_2 = -A_1$, $A_c = 0$ we obtain

$$v_{OUT} = v_d A_d$$

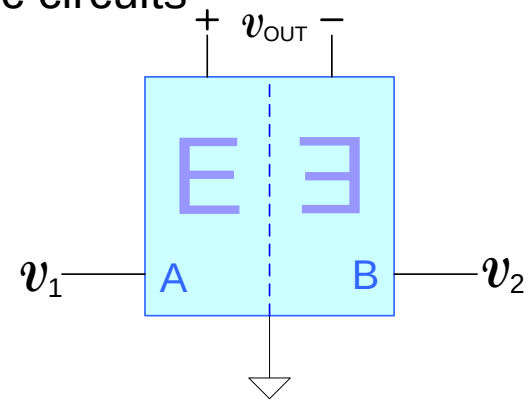
Analysis of op amps up to this point have assumed differential excitation

Common-Mode and Differential-Mode Analysis

Extension to differential outputs and symmetric circuits



Differential Output



Symmetric Circuit with Symmetric Differential Output

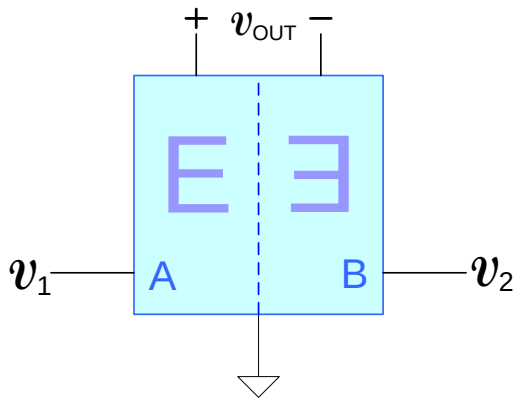
Observation: In a symmetric circuit with a symmetric differential output, $A_C=0$ so can be shown that $v_{OUT}=v_d A_d$ This is summarized in the theorem:

Theorem 2: The symmetric differential output voltage for any symmetric linear network excited at symmetric nodes can be expressed as

$$v_{OUT}=A_d v_d$$

where A_d is the differential voltage gain and the voltage $v_d = v_1 - v_2$

Symmetric Circuit with Symmetric Differential Output



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$$v_{OUT} = A_d v_d$$

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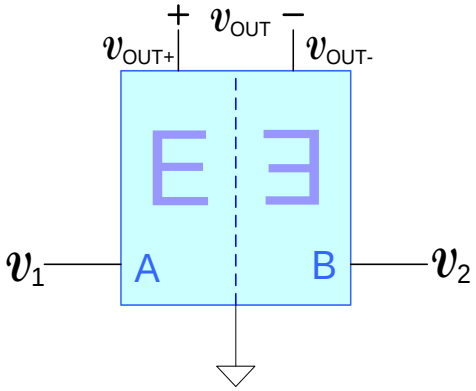
Common-Mode and Differential-Mode Analysis

Proof of Theorem 2 for Symmetric Circuit with Symmetric Differential Output:



By superposition, the single-ended outputs can be expressed as

$$v_{OUT}+ = T_{0PA}v_1 + T_{0PB}v_2$$

$$v_{OUT}- = T_{0NA}v_1 + T_{0NB}v_2$$

where T_{0PA}, T_{0PB}, T_{0NA} and T_{0NB} are the transfer functions from the A and B inputs to the single-ended + and - outputs

taking the difference of these two equations we obtain

$$v_{OUT} = v_{OUT+} - v_{OUT-} = (T_{0PA} - T_{0NA})v_1 + (T_{0PB} - T_{0NB})v_2$$

by symmetry, we have

$$T_{OPA} = T_{ONB} \text{ and } T_{ONA} = T_{OPB}$$

thus can express V_{OUT} as

$$v_{OUT} = (T_{0PA} - T_{0NA})(v_1 - v_2)$$

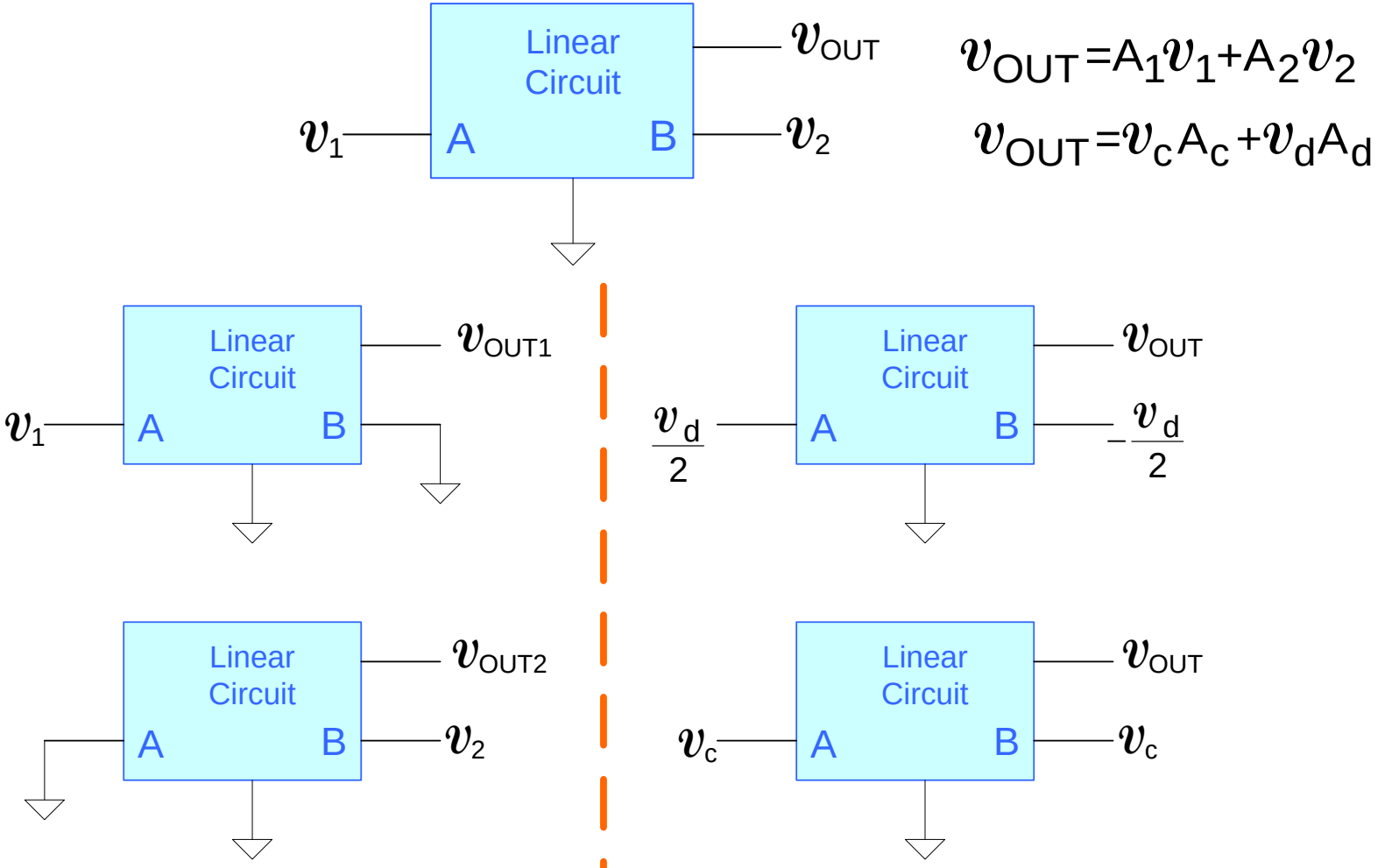
or as

$$v_{OUT} = A_d v_d$$

where $A_d = T_{OPA} - T_{ONA}$ and where $v_d = v_1 - v_2$

Common-Mode and Differential-Mode Analysis

Consider <u>any</u> output voltage for any linear circuit with two inputs



$$v_{OUT} = A_1 v_1 + A_2 v_2$$

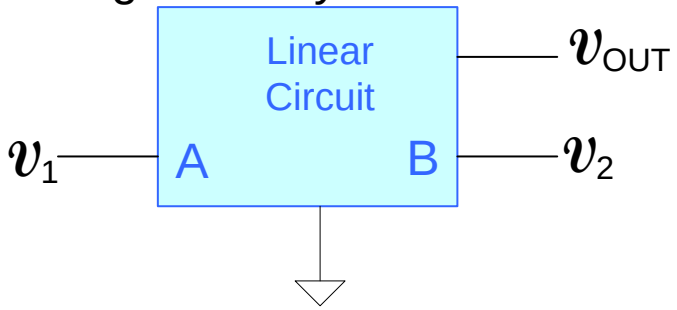
$$v_{OUT} = v_c A_c + v_d A_d$$

Single-Ended Superposition

Difference-Mode/Common-Mode Superposition

Common-Mode and Differential-Mode Analysis

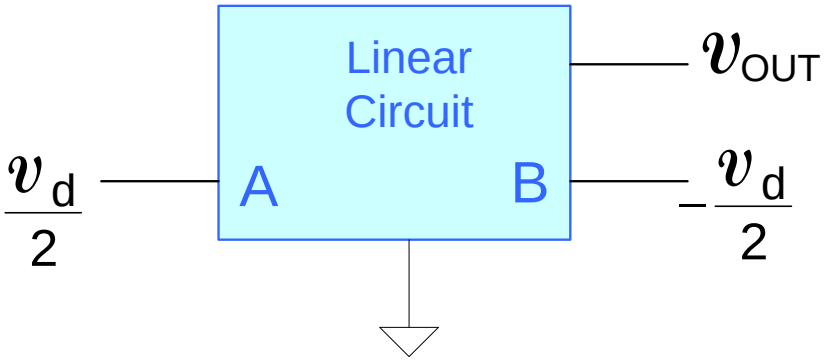
Consider an output voltage for any linear circuit with two inputs

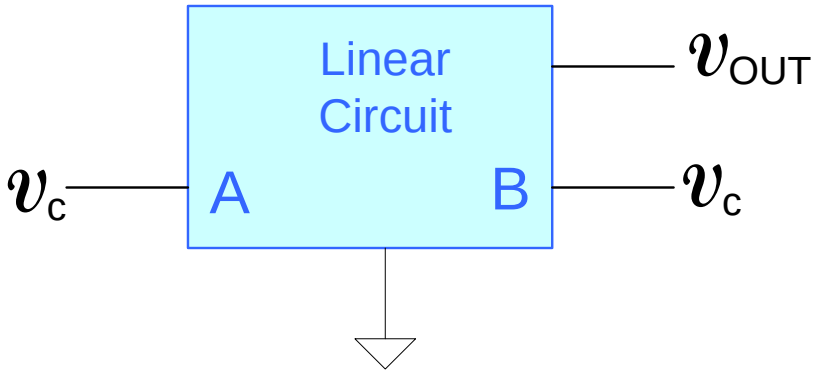


$$v_{OUT} = v_c A_c + v_d A_d$$

- **Difference-Mode/Common-Mode Superposition is almost exclusively used for characterizing Amplifiers that are designed to have a large differential gain and a small common-mode gain**

- **Analysis to this point has been focused only on the circuit on the left**



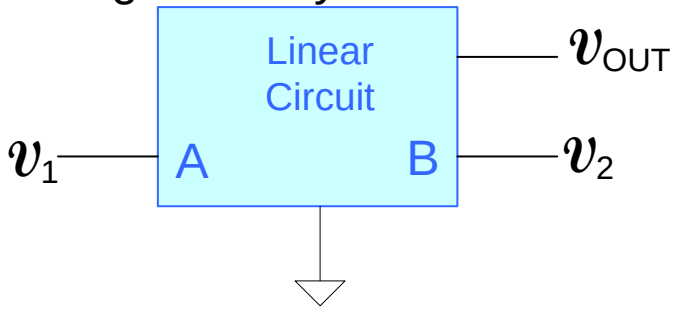


Note: Previous analysis was correct, just did not address whether the circuit had any common mode gain.

Will now get the total output of an amplifier circuit !

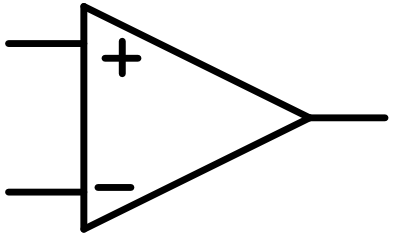
Common-Mode and Differential-Mode Analysis

Consider an output voltage for any linear circuit with two inputs



$$v_{OUT} = v_c A_c + v_d A_d$$

Does Conventional Wisdom Address the Common Mode Gain Issue?



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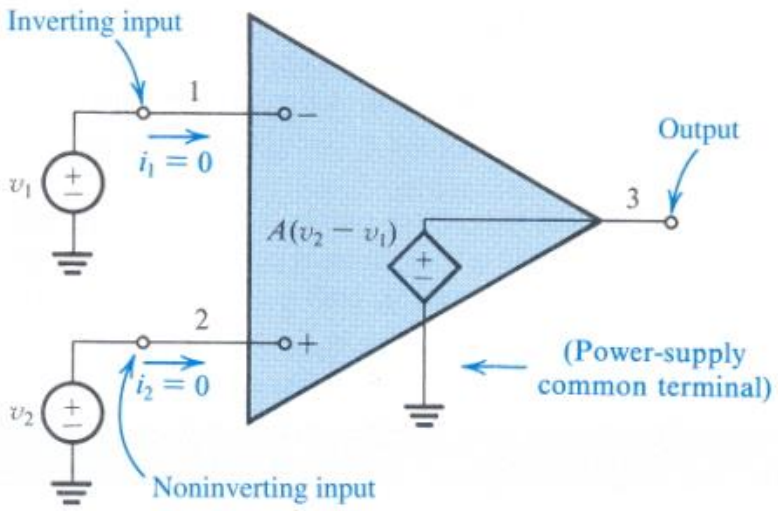


FIGURE 2.3 Equivalent circuit of the ideal op amp.

Yes – Common-Mode Gain was Addressed

Does Conventional Wisdom Address the Common Mode Gain Issue?

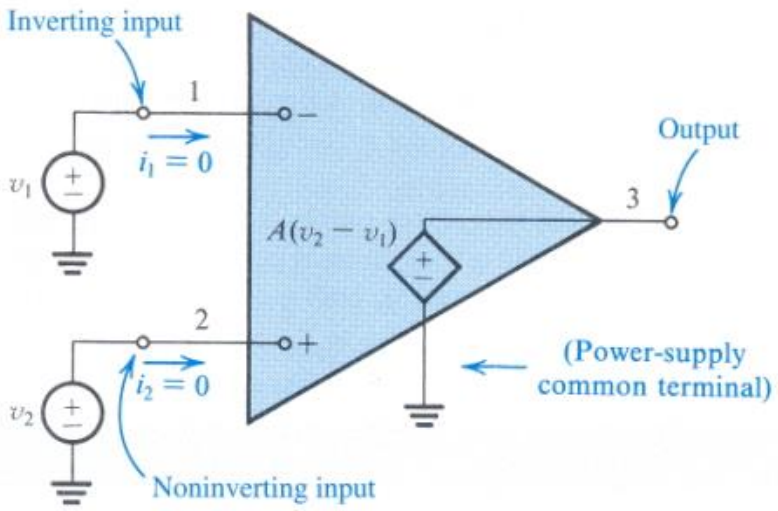


FIGURE 2.3 Equivalent circuit of the ideal op amp.

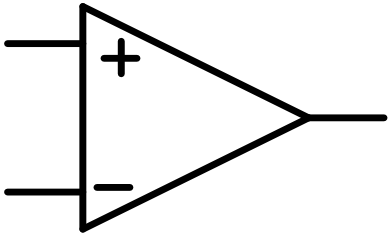
TABLE 2.1 Characteristics of the Ideal Op Amp

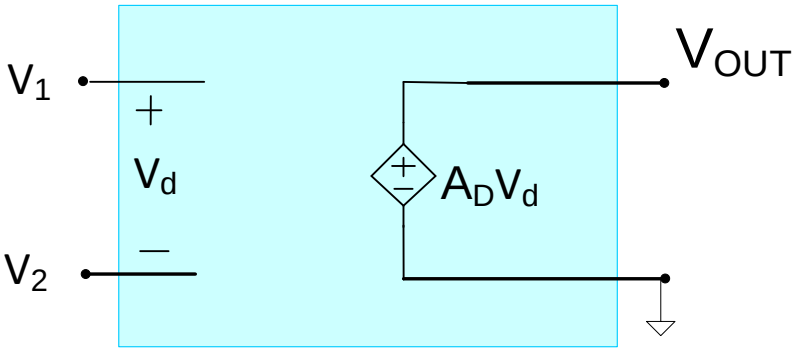
1. Infinite input impedance
2. Zero output impedance
3. Zero common-mode gain or, equivalently, infinite common-mode rejection
4. Infinite open-loop gain A
5. Infinite bandwidth

Yes – Common-Mode Gain was Addressed

How is Common-Mode Gain Modeled?

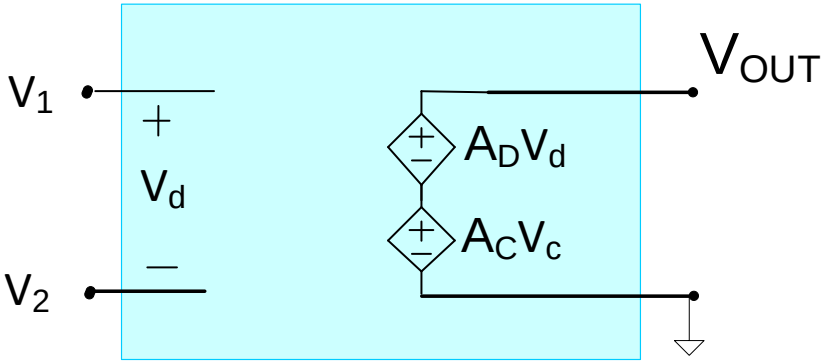
If Op Amp is a Voltage Amplifier with infinite input impedance, zero output impedance, and one terminal of the output is grounded





Ideal Differential Voltage Amplifier

$$V_d = V_1 - V_2$$



Ideal Voltage Amplifier

$$V_d = V_1 - V_2 \qquad V_c = \frac{V_1 + V_2}{2}$$

- Fully Differential Single-Stage Amplifier D
  - General Differential Analysis
  - 5T Op Amp from simple quarter circuit
  - Biasing with CMFB circuit
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  - Overall Transfer Characteristics
- Design of 5T Op Amp
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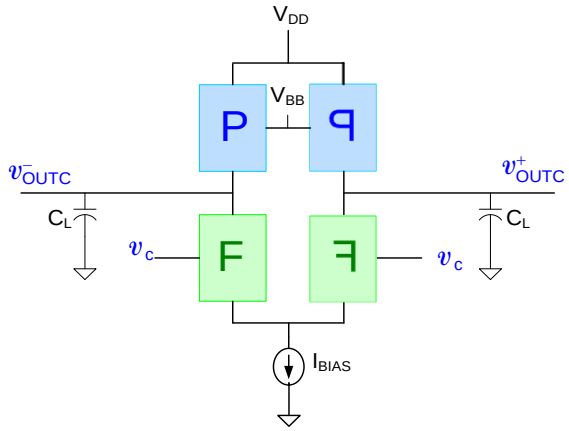
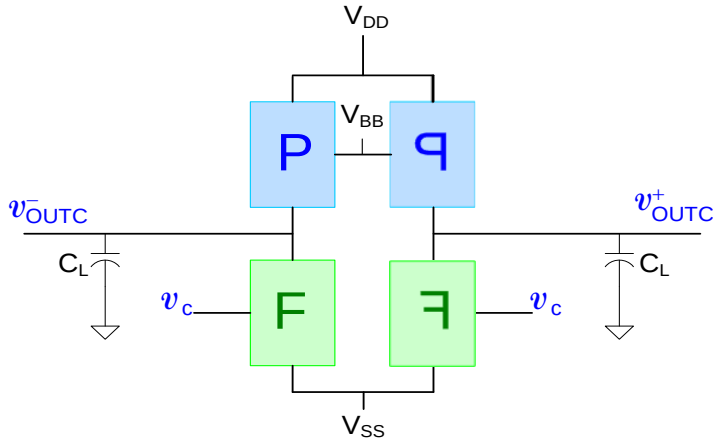
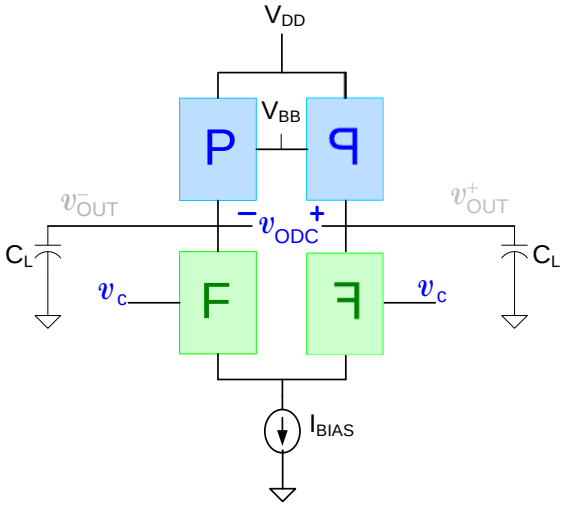
Performance with Common-Mode Input



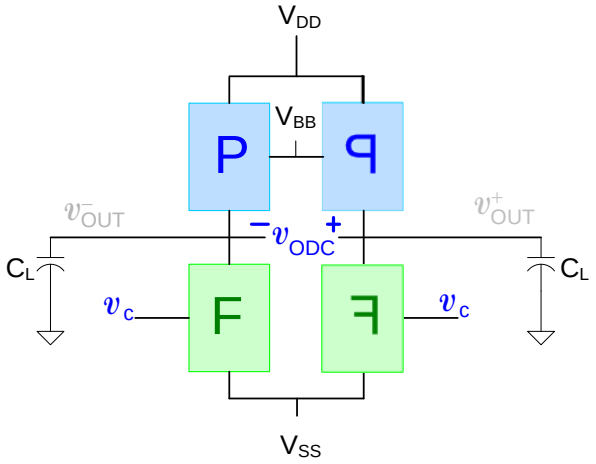
Single-Ended Outputs
Tail-Current Bias



Single-Ended Outputs
Tail-Voltage Bias



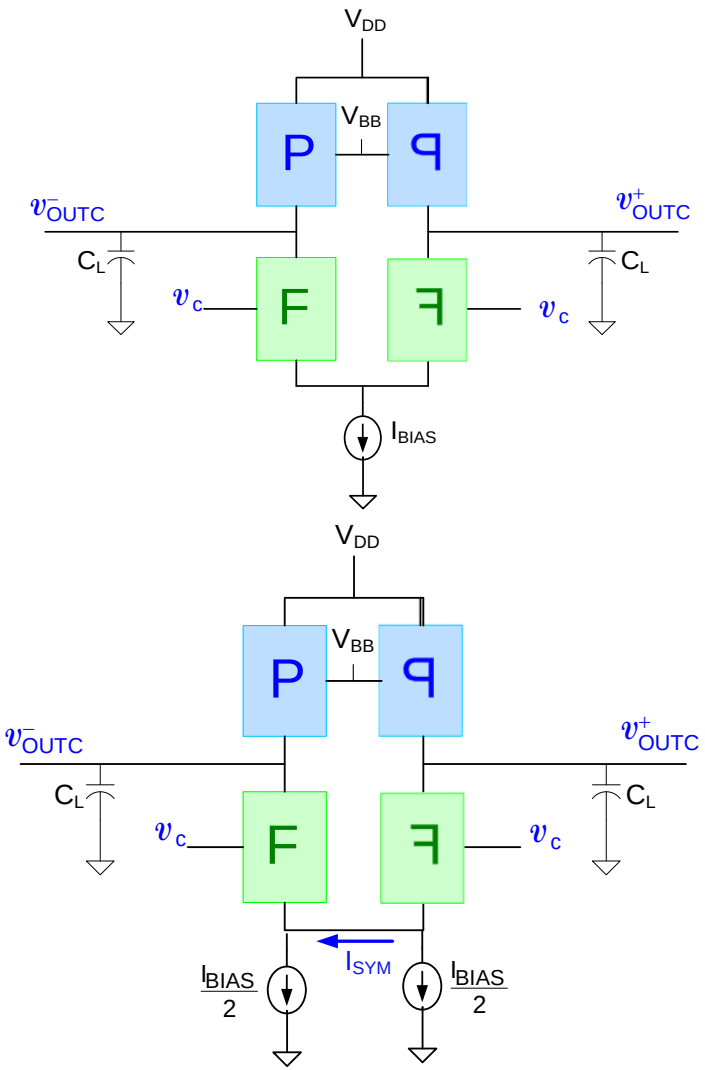
Differential Output
Tail Current Bias



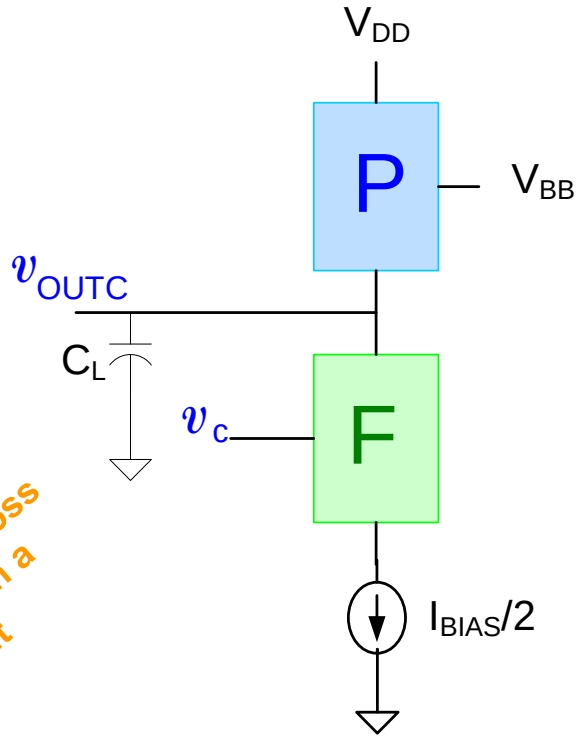
Differential Output
Tail Voltage Bias

Performance with Common-Mode Input

Consider tail-current bias amplifier



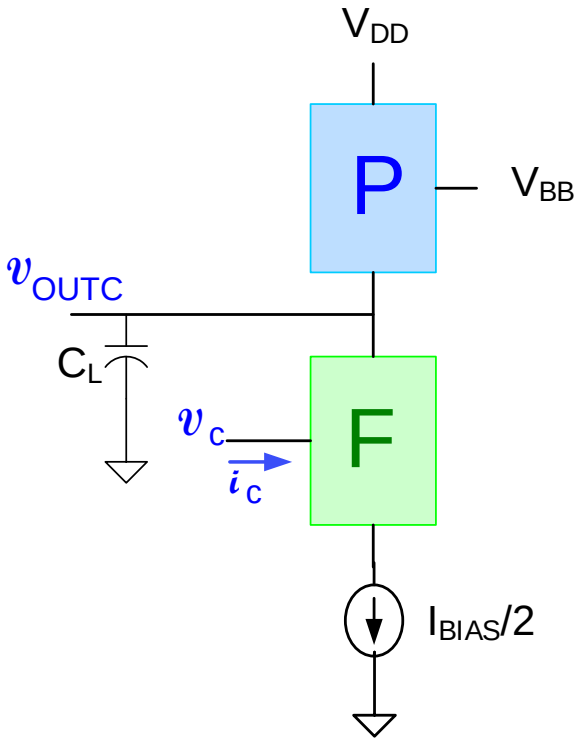
No current flows across axis of symmetry in a symmetric circuit



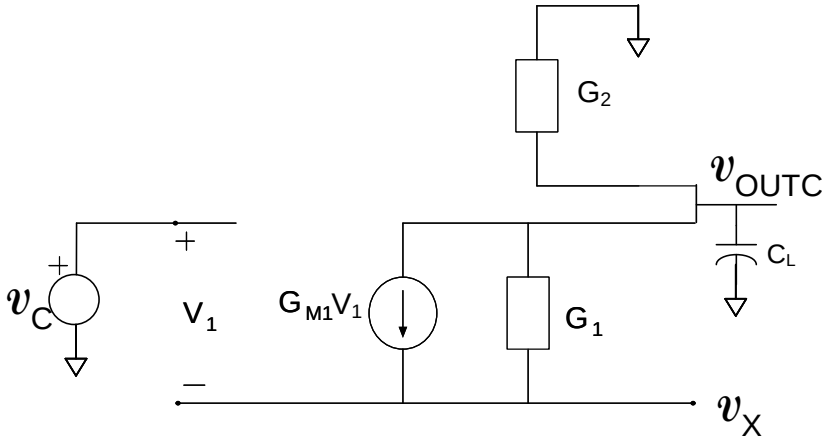
Common-Mode Half-Circuit

Performance with Common-Mode Input

Consider tail-current bias amplifier with i_c=0



Common-Mode Half-Circuit



$$v_{OUTC}(sC+G_1+G_2)+G_{M1}v_1 = G_1 v_X$$
$$v_C = v_1+v_X$$
$$v_X G_1 - G_{M1}v_1 = v_{OUTC}\, G_1$$

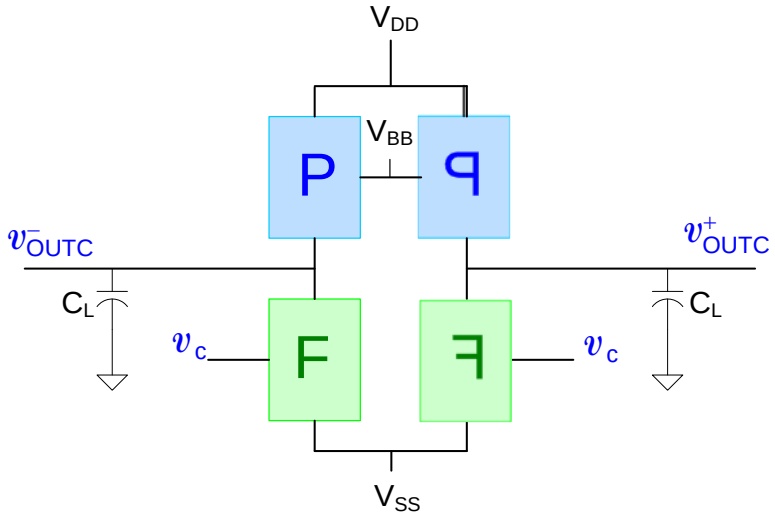
Solving, we obtain

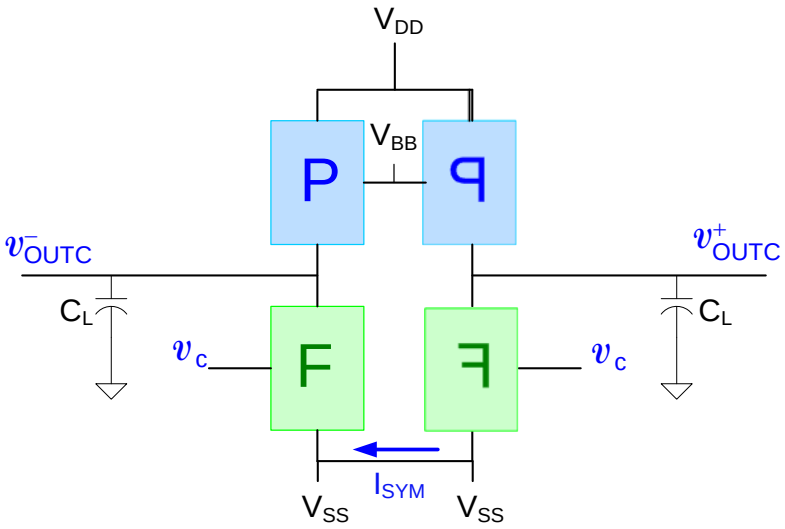
v_{OUTC}=0 thus A_C=0

(Note: Have assumed an ideal tail current source in this analysis A_C will be small but may not vanish if tail current source is not ideal. Analysis with nonideal current source is simple)

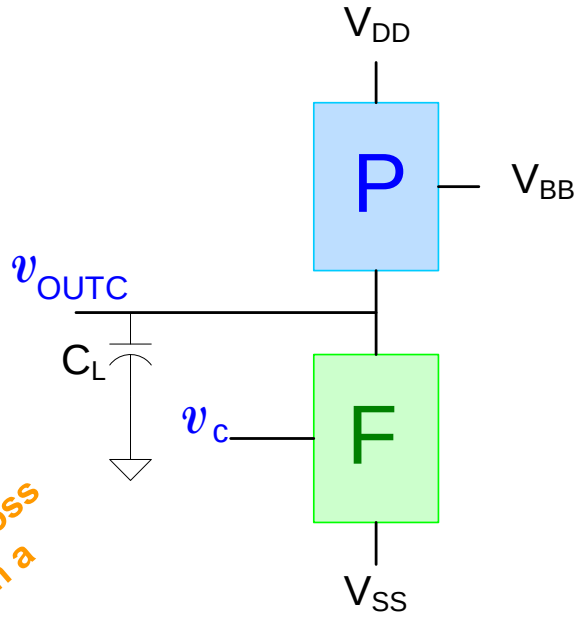
Performance with Common-Mode Input

Consider tail-voltage bias amplifier with i_c=0





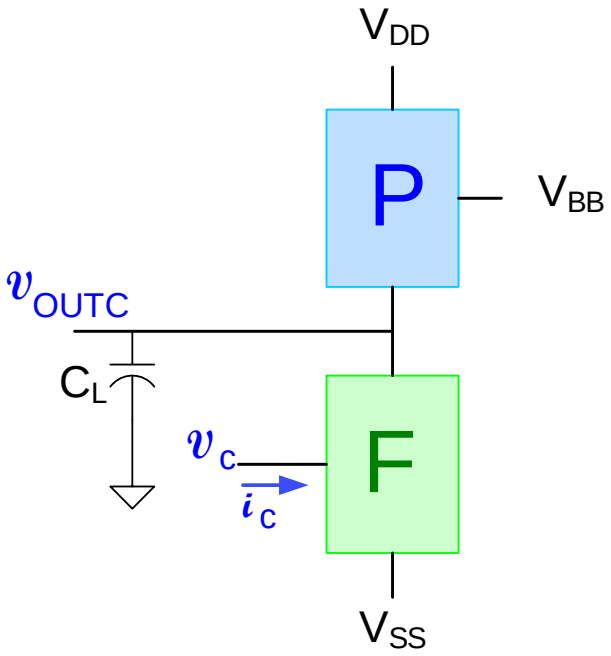
No current flows across axis of symmetry in a symmetric circuit



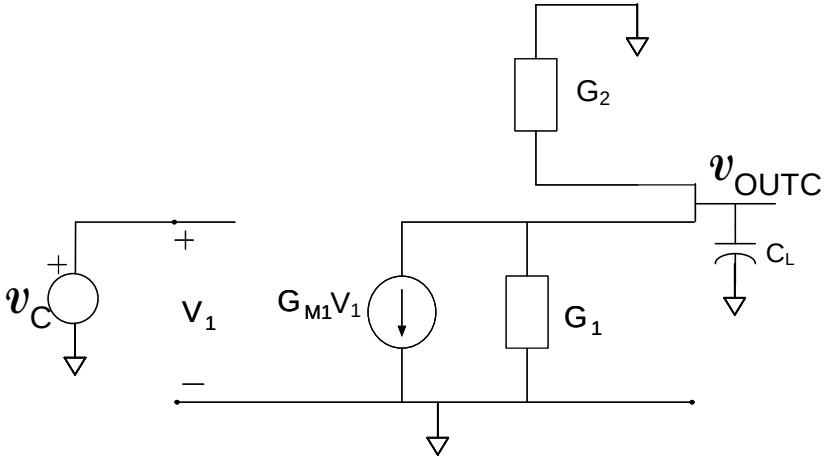
Common-Mode Half-Circuit

Performance with Common-Mode Input

Consider tail-voltage bias amplifier with i_c=0



Common-Mode Half-Circuit



$$\left.\begin{aligned} v_{OUTC}(sC+G_1+G_2)+G_{M1}v_1 &= 0 \\ v_C &= v_1 \end{aligned}\right\}$$

Solving, we obtain

$$\frac{v_{OUTC}}{v_C} = A_C = \frac{-G_{M1}}{sC+G_1+G_2}$$

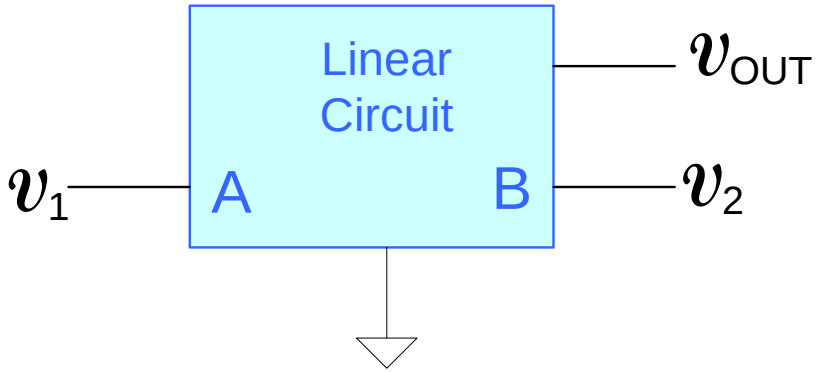
This circuit has a rather large common-mode gain and will not reject common-mode signals

- Not a very good differential amplifier
- But of no concern in applications where v_C=0

- Fully Differential Single-Stage Amplifier D
  - General Differential Analysis
  - 5T Op Amp from simple quarter circuit
  - Biasing with CMFB circuit
  - Common-mode and differential-mode analysis
  - Common Mode Gain
  - Overall Transfer Characteristics
- Design of 5T Op Amp
- Slew Rate

Overall Small-Signal Analysis

As stated earlier, with common-mode gain and difference-mode gains available



$$v_{OUT} = v_c A_c + v_d A_d$$

- Fully Differential Single-Stage Amplifier D
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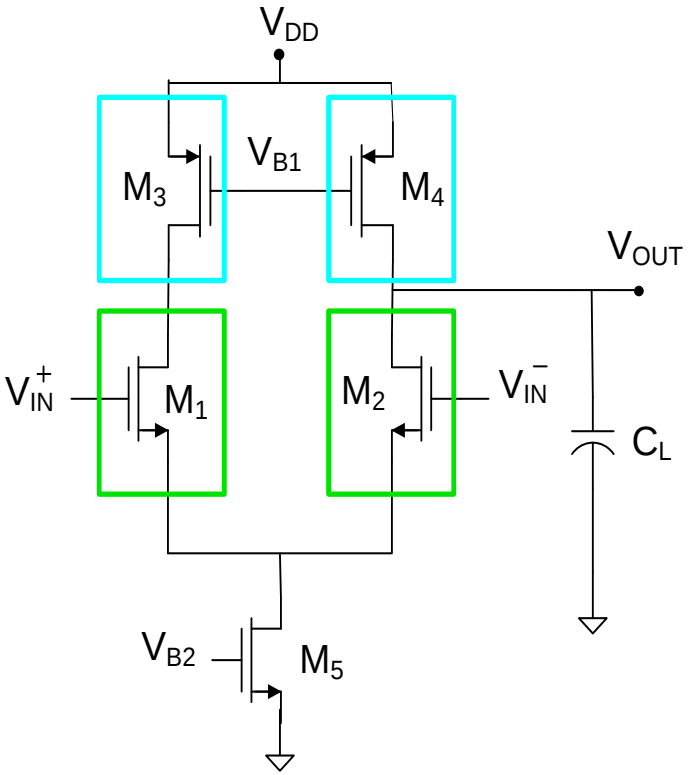
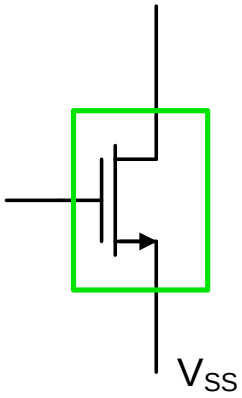
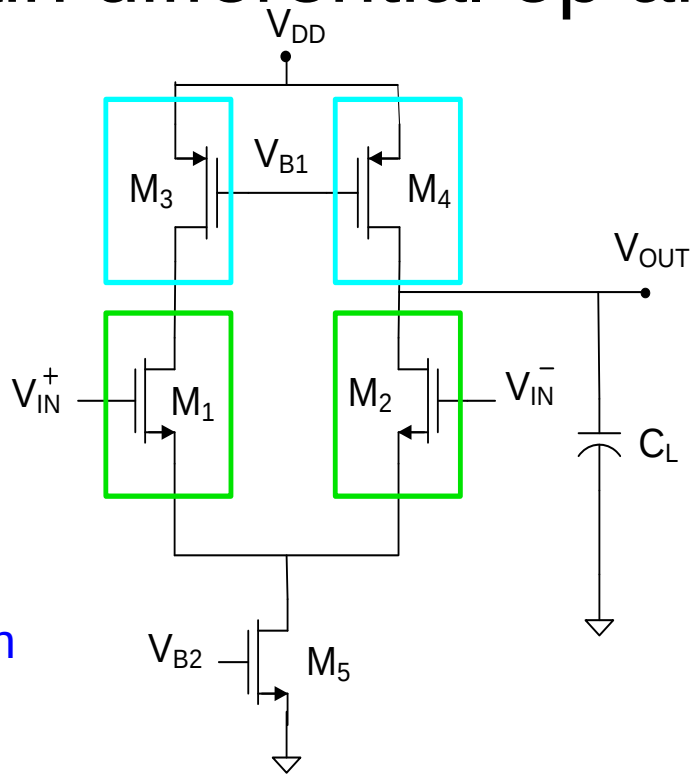
Design of 5T op amp



Single-stage low-gain differential op amp



Quarter Circuit



Single-Ended Output : Differential Input Gain

$$A(s) = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{O1} + g_{O3}}$$

$$A_o = \frac{\frac{g_{m1}}{2}}{g_{O1} + g_{O3}}$$

$$GB = \frac{g_{m1}}{2C_L}$$

Need a CMFB circuit to establish V_{B1}

Design of Basic Single-stage low-gain differential op amp

$$A(s) = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{O1} + g_{O3}}$$

$$A_o = \frac{\frac{g_{m1}}{2}}{g_{O1} + g_{O3}}$$

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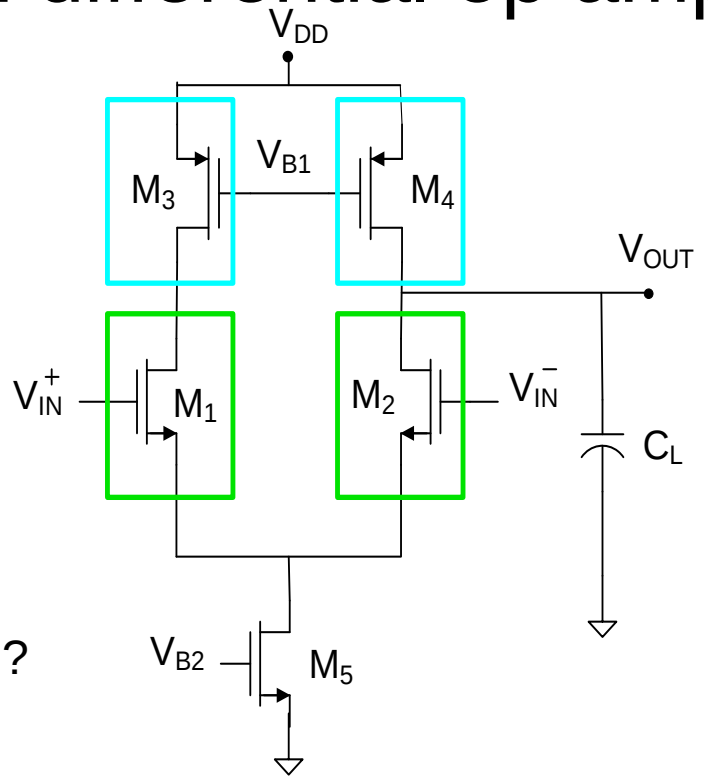


What are the number of degrees of freedom?
(assume V_{DD}, C_L fixed, Symmetry)

Natural Parameters (assuming symmetry):

$$\left\{\frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, V_{B1}, V_{B2}\right\}$$

Constraints: $I_{D5} \simeq 2I_{D3}$

Net Degrees of Freedom: 4

Need a CMFB circuit to establish V_{B1}

- Expressions for A_0 and GB were obtained from quarter-circuit
- Expressions for A_0 and GB in terms of natural parameters for quarter circuit were messy
- Can show that expressions for A_0 and GB in terms of natural parameters for 5T amplifier are also messy

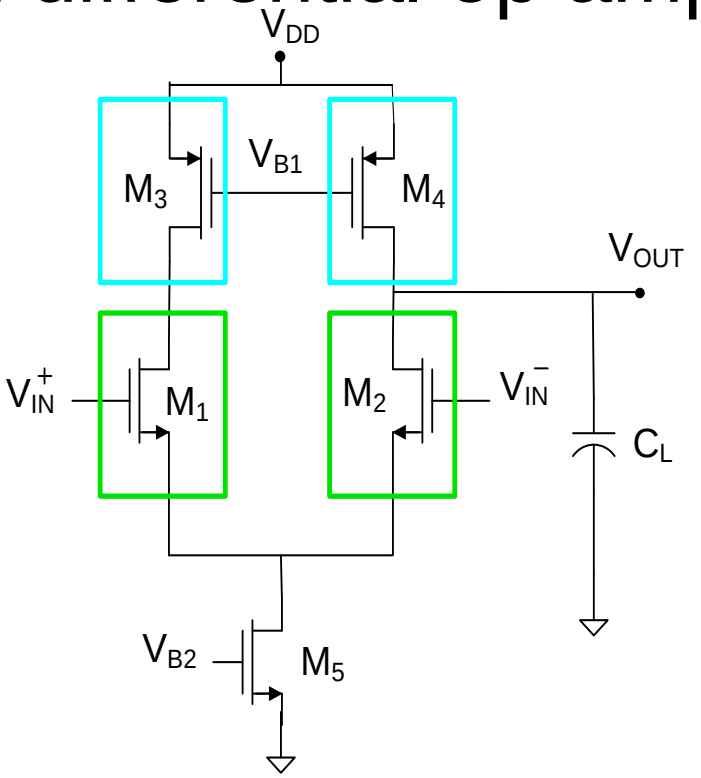
Can a set of practical design parameters be identified?

Design of Basic Single-stage low-gain differential op amp

$$A(s) = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{O1} + g_{O3}}$$

$$A_o = \frac{\frac{g_{m1}}{2}}{g_{O1} + g_{O3}}$$

$$GB = \frac{g_{m1}}{2C_L}$$



What are the number of degrees of freedom?
(assume V_{DD}, C_L fixed, Symmetry)

Need a CMFB circuit to establish V_{B1}

Natural Parameters:

$$\left\{\frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, V_{B1}, V_{B2}\right\}$$

Constraints: $I_{D5} \simeq 2I_{D3}$

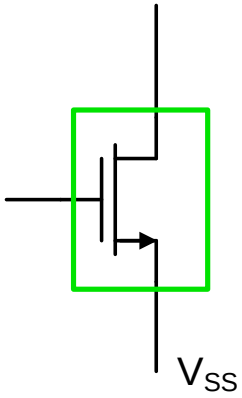
Net Degrees of Freedom: 4

Practical Parameters:

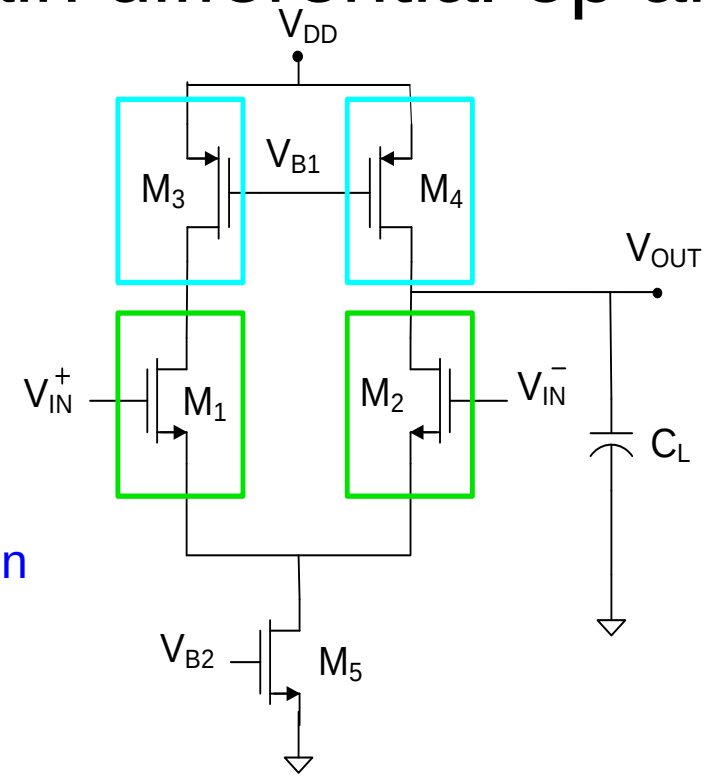
$$\{V_{EB1}, V_{EB3}, V_{EB5}, P\}$$

Will now express performance characteristics in terms of Practical Parameters

Design of Basic Single-stage low-gain differential op amp



Quarter Circuit



Single-Ended Output : Differential Input Gain

$$A(s) = \frac{-\frac{g_{m1}}{2}}{sC_L + g_{O1} + g_{O3}}$$

$$A_o = \frac{\frac{g_{m1}}{2}}{g_{O1} + g_{O3}}$$

$$GB = \frac{g_{m1}}{2C_L}$$

$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{1}{V_{EB1}}\right) \qquad GB = \left(\frac{P}{V_{DD}C_L}\right) \bullet \left[\frac{1}{2V_{EB1}}\right]$$

Practical Parameters:

$$\{V_{EB1}, V_{EB3}, V_{EB5}, P\}$$

Have 4 degrees of freedom but only two practical variables impact A_0 and GB so still have 2 DOF after meet A_0 and GB requirements

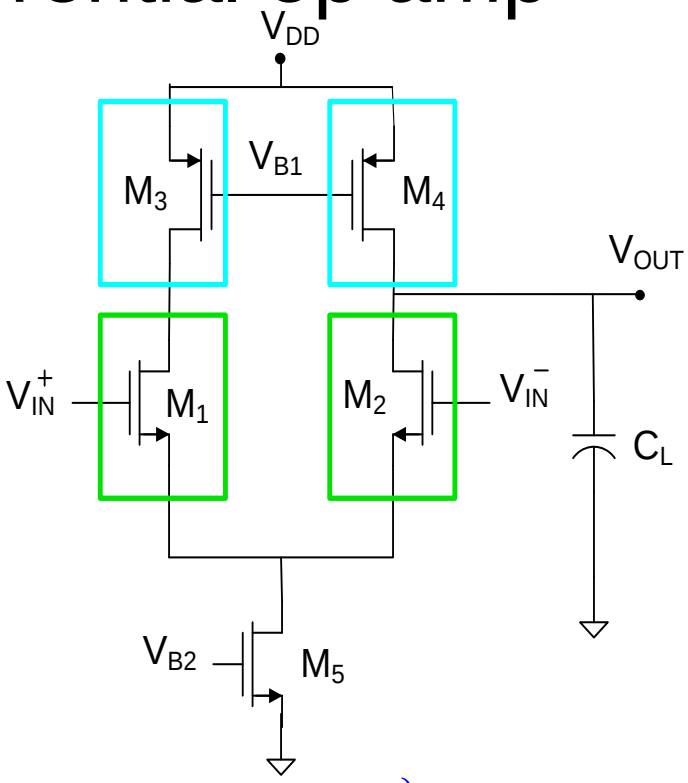
Need a CMFB circuit to establish V_{B1}

Design of Basic Single-stage low-gain differential op amp

Single-Ended Output : Differential Input Gain

Practical Parameters: $\{V_{EB1}, V_{EB3}, V_{EB5}, P\}$

$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{1}{V_{EB1}}\right) \qquad GB = \left(\frac{P}{V_{DD}C_L}\right) \bullet \left[\frac{1}{2V_{EB1}}\right]$$



Design Strategy with fixed A_0 and GB requirements:

1. Pick V_{EB1} to meet gain requirements
2. Pick P to meet GB requirements
3. Pick V_{EB3} and V_{EB5} to achieve other desirable properties (i.e. explore the remaining part of the design space)

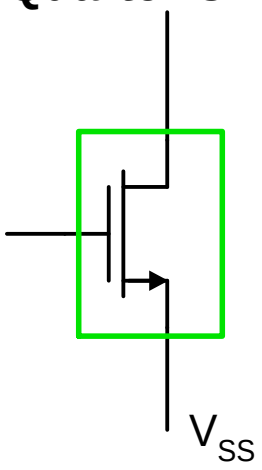
$\{\cancel{V_{EB1}}, V_{EB3}, V_{EB5}, P\}$

$\{\cancel{V_{EB1}}, V_{EB3}, V_{EB5}, \cancel{P}\}$

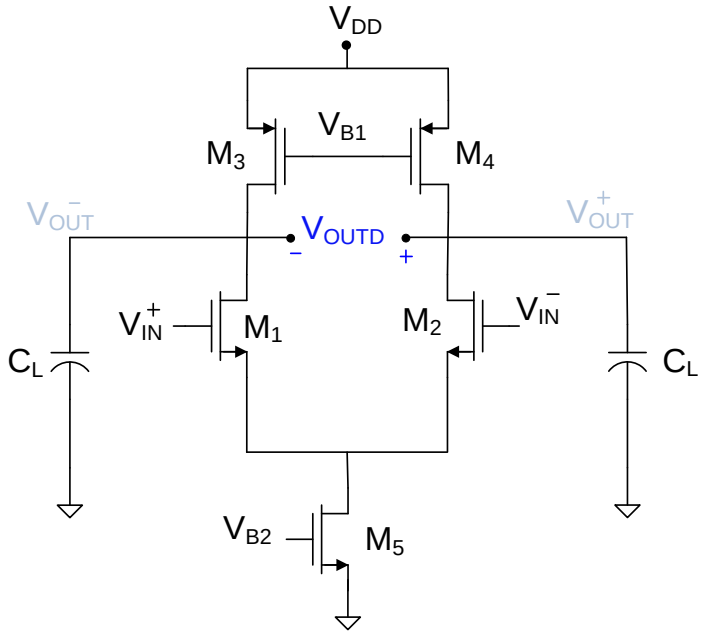
Note: Design strategy may change if A_0 and GB are not firm requirements

Single-stage low-gain differential I/O op amp

Quarter Circuit



$$V_{OD} = V_O^+ - V_O^-$$



Differential Output : Differential Input Gain

$$A(s) = \frac{g_{m1}}{sC_L + g_{O1} + g_{O3}}$$

$$A_O = \frac{g_{m1}}{g_{O1} + g_{O3}}$$

$$GB = \frac{g_{m1}}{C_L}$$

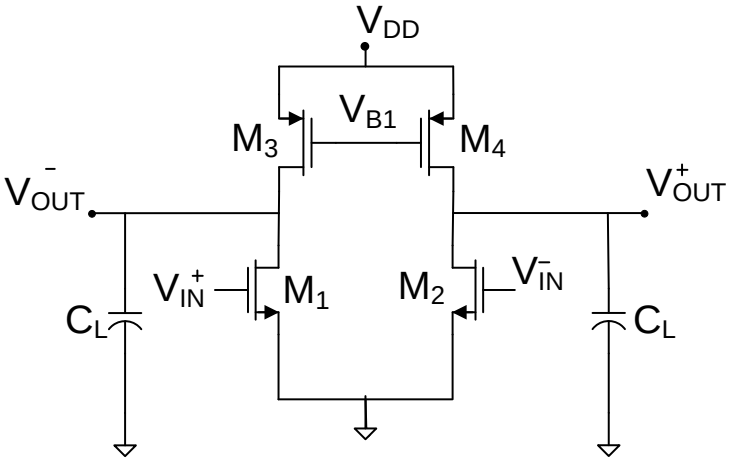
$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{2}{V_{EB1}}\right) \qquad GB = \left(\frac{P}{V_{DD}C_L}\right) \bullet \left[\frac{1}{V_{EB1}}\right]$$

Have 4 degrees of freedom but only two practical variables impact A_0 and GB so still have 2 DOF after meet A_0 and GB requirements that can be used for other purposes

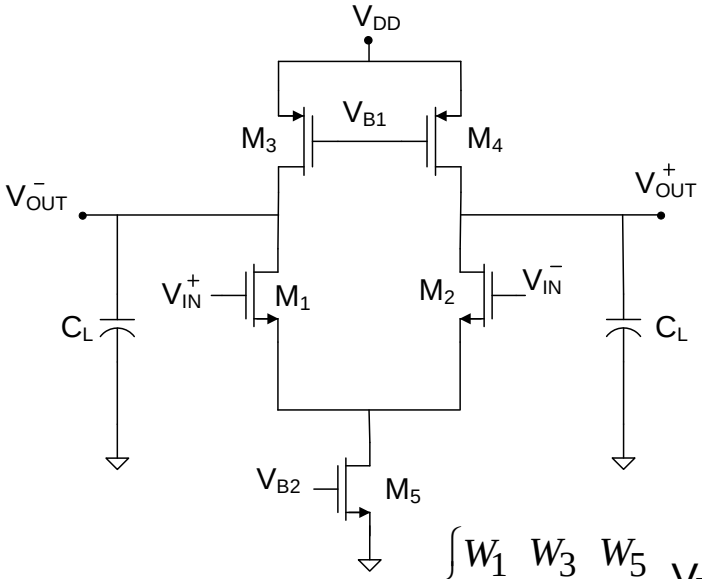
Need a CMFB circuit to establish V_{B1} or V_{B2}

A_D expressions valid for both tail-current and tail-voltage op amp

Recall:



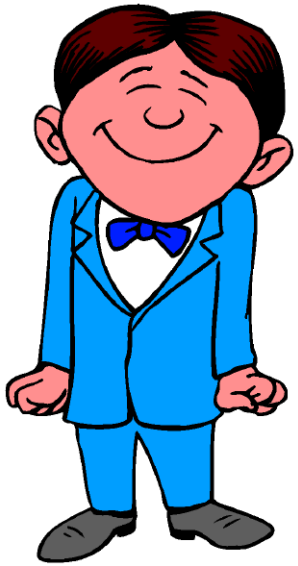
$$\left\{\frac{W_1}{L_1}, \frac{W_3}{L_3}, V_{B1}\right\}$$



$$\left\{\frac{W_1}{L_1}, \frac{W_3}{L_3}, \frac{W_5}{L_5}, V_{B1}, V_{B3}\right\}$$

So which one should be used?

- Common-mode input range large for tail current bias
- Improved rejection of common-mode signals for tail current bias
- Two extra design degree of freedom for tail current bias
- Improved output signal swing for tail voltage bias (will show later)



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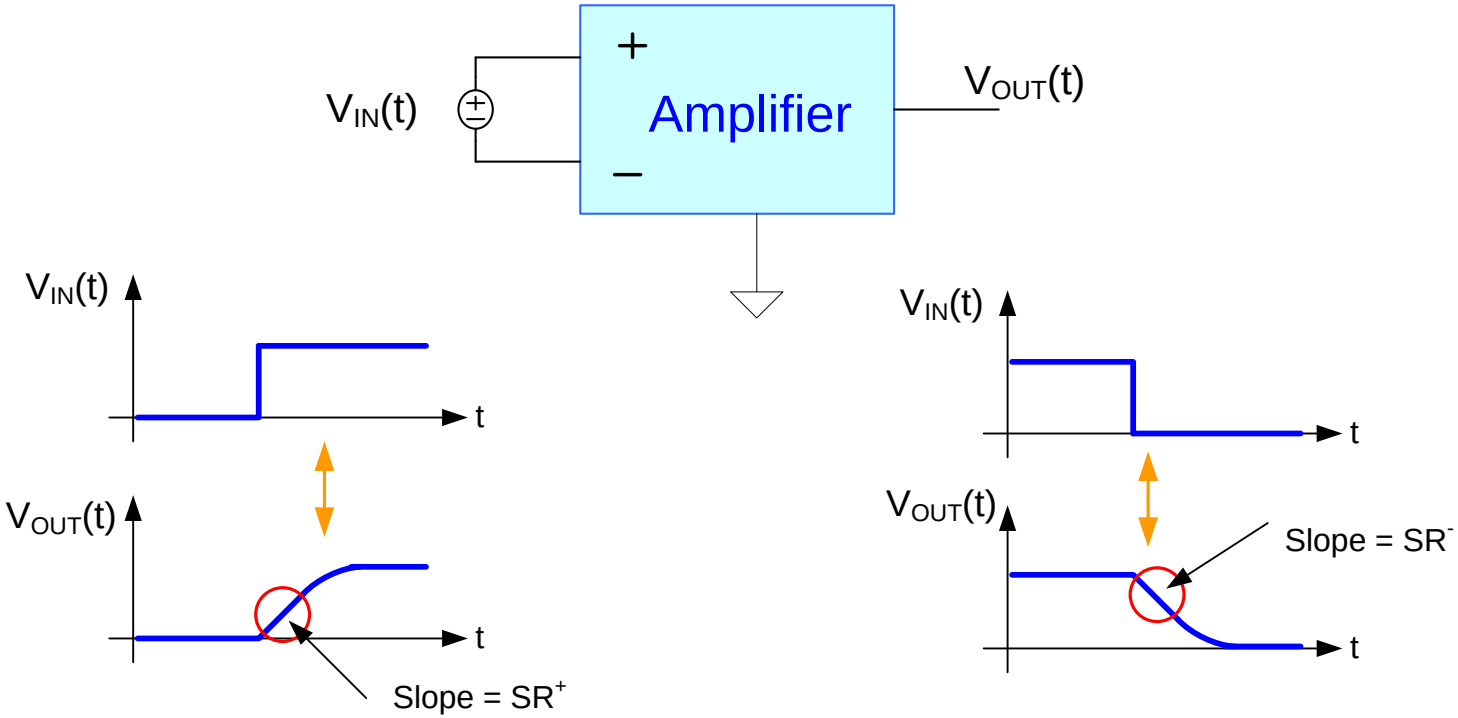
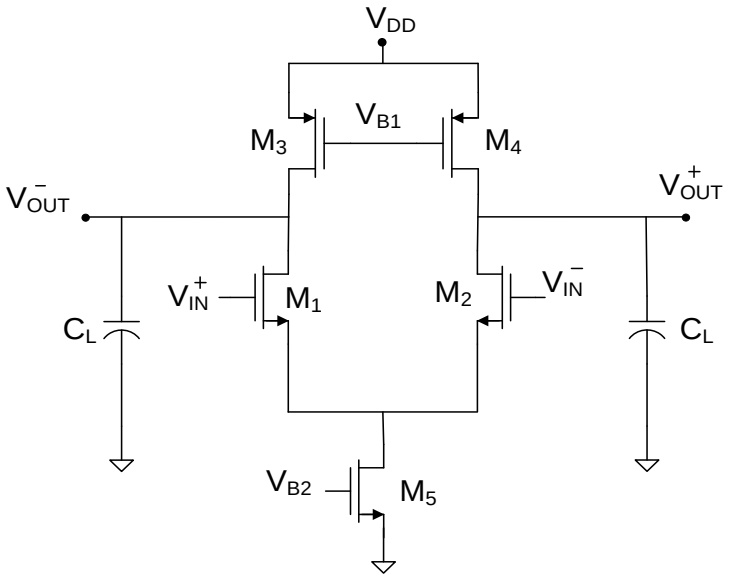
Slew Rate

Definition: The slew rate of an amplifier is the maximum rate of change that can occur at the output node



- SR is a nonlinear large-signal characteristic
- Input is over-driven (some devices in amplifier usually leave normal operating region)
- Hard input overdrive depicted in this figure
- Magnitude of SR^+ and SR^- usually same and called SR (else SR^+ and SR^- must be given)

Slew Rate for 5T Op Amp



With large step input on V_{IN}^+, all tail current (I_T) will go to M_1 thus turning off M_2 thus current through M_4 which is ½ of I_T will go to load capacitor C_L

The I-V characteristics of any capacitor is

$$I=C\frac{dV}{dt}$$

Substituting $I=I_T/2$, $V=V_{OUT}^+$ and $C=C_L$ obtain a voltage ramp at the output thus

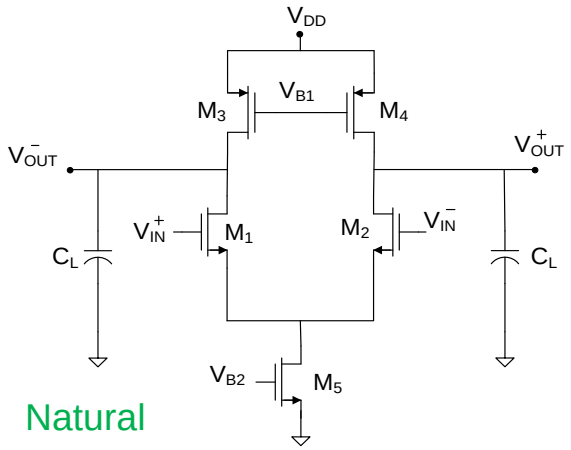
$$SR^+=\frac{dV_{OUT}^+}{dt}=\frac{I_T}{2C_L}$$

Natural parameter domain

$$SR^+=\frac{P}{V_{DD}2C_L}$$

Practical parameter domain

Slew Rate for 5T Op Amp



$$SR^+ = \frac{I_T}{2C_L}$$

Natural parameter domain

$$SR^+ = \frac{P}{V_{DD}2C_L}$$

Practical parameter domain

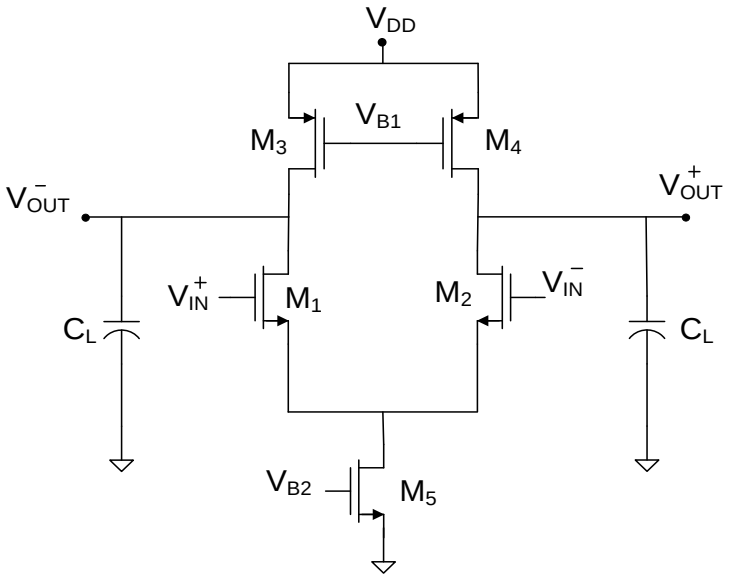
Question: Can SR^+ be expressed as product of model parameters and architecture dependent term?

$$SR^+ = \left[\frac{1}{2C_L}\right][I_T] \qquad SR^+ = \left[\frac{1}{V_{DD}2C_L}\right][P]$$

Question: Can SR^+ be expressed in small-signal parameter domain?

$$SR^+ = \frac{g_{o1}I_T}{\lambda 2C_L} = \left[\frac{I_T}{\lambda 2C_L}\right][g_{o1}]$$

Slew Rate



It can be similarly shown that putting a large negative step on the input steer all current to M_2 thus the current to the capacitor C_L will be I_T minus the current from M_2 which is still $I_T/2$. This will cause a negative ramp voltage on V_{OUT}^+ of value

$$SR^- = \frac{dV_{OUT}^+}{dt} = -\frac{I_T}{2C_L} = -\frac{P}{V_{DD}2C_L}$$

Since the magnitude of SR^+ and SR^- are the same, obtain a single SR for the amplifier of value

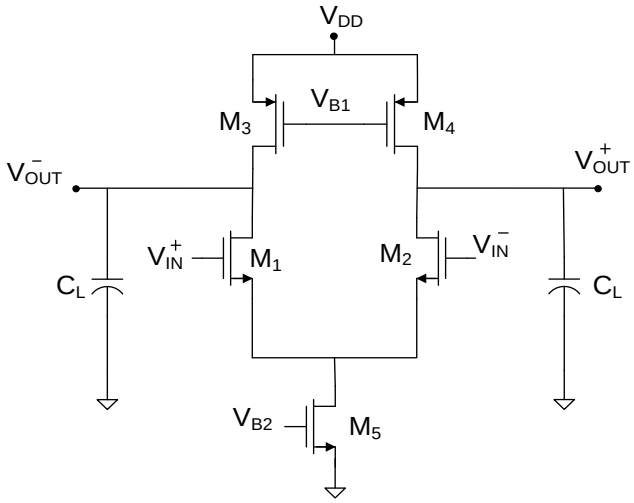
$$SR = \frac{P}{V_{DD}2C_L}$$

Interdependence of Parameters

$$A_0 = \left[\frac{1}{\lambda_1 + \lambda_3}\right]\left(\frac{1}{V_{EB1}}\right)$$

$$GB = \left(\frac{1}{2V_{DD}C_L}\right) \bullet \left[\frac{P}{V_{EB1}}\right]$$

$$SR = \frac{P}{V_{DD}2C_L}$$



Note: With this structure, the three key performance characteristics {A_0, GB, SR} can not be independently specified

e.g. If V_{EB1} is picked to set A_0, then $\frac{P}{V_{DD}C_L}$ will determine both GB and SR

Alternately, observe $SR = \frac{GB}{A_0(\lambda_1+\lambda_2)}$

Stay Safe and Stay Healthy !

End of Lecture 4